Development of Millimeter Wave Multi-layer Organic Based MCM Technology

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Abstract

We present the design and development of multi-layer organic based MCM's for use at millimeter wave frequencies. In this technology, we utilize a multi-layer interconnect using a vertical stacked via process. We experimentally develop and analyze an equivalent circuit model for this multi-layer interconnect to millimeter wave frequencies. We demonstrate that this vertical interconnect has ultra low parasitics and can be used to realize high performance modules at millimeter wave frequencies.

Introduction

The driving forces behind the development of new packaging approaches are the reduction of size, weight and improvement of functionality. Conventionally, wire bonds are used to connect components and IC on a ceramic substrate that are housed in a module. However, wire bonds are inherently a primary source of parasitics, especially at millimeter wave frequencies. The use of wire bonds is not effective and feasible to realize compact modules since the parasitics introduced significantly degrade the performance of the entire module. In this paper, we present the use of overlay dielectric films with ICs embedded in recesses [3-7]. This 3-D packaging approach offers very low parasitic interconnects and compact modules. In addition, the HDI technology developed by GE/Lockheed Martin has passed MIL-STD-883 and space qualification requirements. With this proven reliability, HDI technology has been inserted into a variety of space and military applications, including GE-1, GE-2 and GE-3 communications satellites.

In this paper, we experimentally study and analyze the performance of the vertical stacked via interconnect. We experimentally develop the electrical model for the stacked via to 50 GHz [6]. This ultra low parasitic vertical interconnect transitions between microstrip line and stripline structures in various dielectric layers to IC's in cavities. We compare the characteristics of the vertical stacked via interconnect with wirebond and flip-chip to investigate their relative performance. We demonstrate that the return loss of two 50-Ω transmission lines connected by the vertical stacked via achieves less than 20 dB return loss to 50 GHz. In this paper, we demonstrate an alternative to flip chip vertical interconnect for use in multi-chip modules.

Multi-layer Packaging Concept

The High Density Interconnect (HDI) MCM is a chip first approach where ICs are placed in cavities formed in a ceramic or plastic substrate [1,2]. Interconnect layers are formed above the IC's where vertical stacked vias are

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used to make contact with the pads of the ICs housed in ceramic cavities. Ti/Cu/Ti is the metalization for the multi-layer interconnects. The interconnect layer is usually composed of three layers, with each layer consisting of an adhesive and a polymer dielectric. The initial layer is composed of Ultem® (a trademark of General Electric) adhesive, a thermoplastic polyetherimide, and a Kapton E® (a trademark of DuPont) dielectric film. The second and third layers are composed of either a siloxane polyimide/epoxy (SPIE) blend adhesive or a thermoset polymer (benzocyclobutene (BCB)) with a Kapton E® dielectric film. The adhesive thicknesses range from 11 to 13 microns and the dielectric film thicknesses range from 22 to 24 microns. A typical multi-layer organic interconnect cross-section is shown in Figure 1.

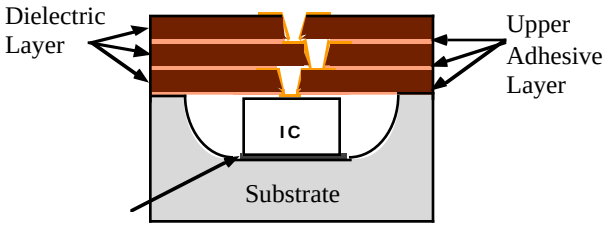


Figure 1. A cross-section of the multi-layer organic based MCM

Vertical interconnects

We have designed various microstrip transmission lines on three-layers of Kapton E® with adhesives as shown in Figures 2a and 2b. The dielectric data of the polymer and adhesive is found in [3]. The total dielectric thickness including Kapton E® and adhesives is 102 µm. The microstrip transmission lines have coplanar waveguide (CPW) launches. These launches are connected to ground using vertical stacked vias. These stacked vias represent the vertical interconnects to an IC in a cavity as shown in Figure 1.

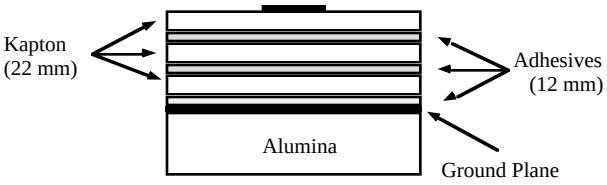


Figure 2a. A cross-section of a microstrip line on multi-layer structure

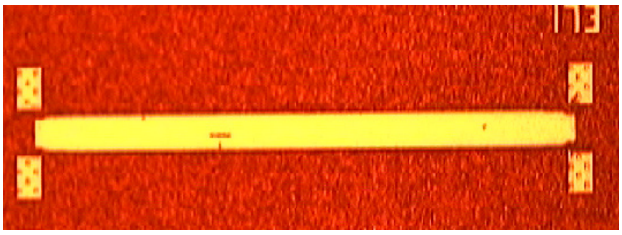


Figure 2b. A microstrip transmission line with vertical interconnects at both ends

We use an HP85109C network analyzer (ANA), coplanar waveguide microprobes and a Cascade Microtech probe station to obtain S-parameters. We perform an on-wafer Thru-Reflect-Match calibration on an Impedance Standard Substrate (ISS). We then measure various microstrip transmission lines (Figure 3) which include vertical stacked vias for the ground pads of the coplanar launches. In Figure 3, we show the insertion loss of 50-Ω microstrip transmission lines on polymers and alumina dielectric substrate. The loss performance of the 50-Ω microstrip transmission line on Kapton and BCB is comparable to that of the microstrip transmission line on a 5-mil thick alumina substrate at W-band (75GHz-110GHz). We develop an equivalent circuit model for the vertical interconnect as shown in Figure 4. The L_g, C_1 and C_2 represent the inductance and fringing capacitance of the vertical stacked via. We use the Hewlett-Packard's Microwave Design System to optimize this circuit until the measured and modeled results are well correlated as shown in Figure 5.

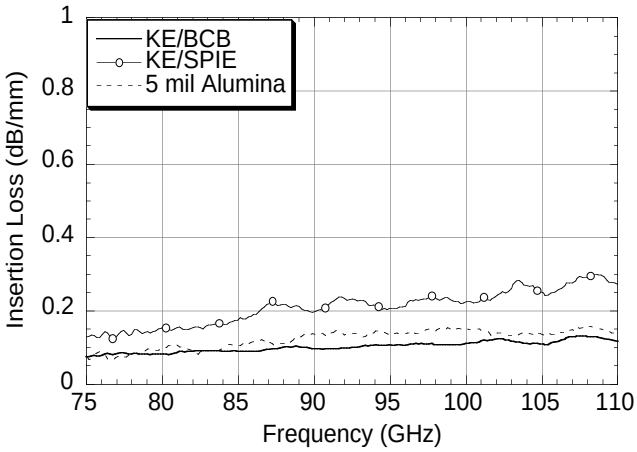


Figure 4. Insertion loss versus frequency data for the following three types of microstrip lines: (1) multi-layer 50-Ω microstrip with Kapton E dielectric and BCB adhesive (KE/BCB), (2) multi-layer 50-Ω microstrip with Kapton E dielectric and SPIE (KE/SPIE), and (3) 50-Ω microstrip on 5 mil thick alumina

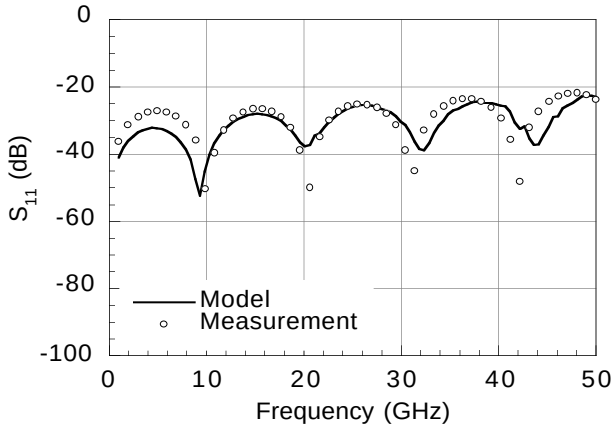
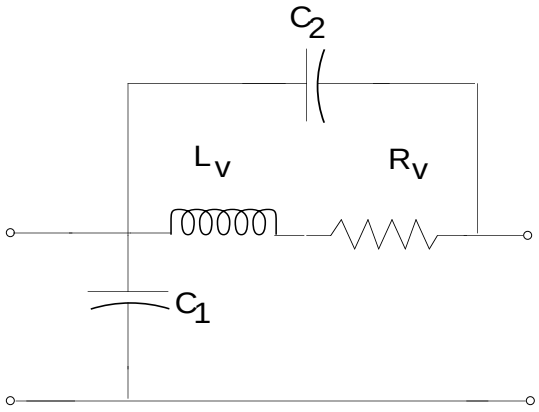


Figure 5. Measured and modeled S_{11} of the 50-Ω microstrip line with the vertical stacked via interconnect



L_v = 55 fH, C_1 = 10 fF, C_2 = 9.3 fF, R_v = 0.1 Ω

Figure 6. The equivalent circuit model of the vertical interconnect

We compare the return loss of our interconnect to that of bond wires. The data for the bond wires is reported in [7]. In Table 1, we show that the vertical stacked via interconnect has ultra low parasitics and provides an excellent match. To evaluate its performance, we design a test structure connecting a 50-Ω microstrip line to a 50-Ω stripline using the vertical stacked via as shown in Figure 6. In Figure 7, we achieve the measured return loss of less than 20dB for this structure to 50GHz. We compare the return loss of our structure with one using flip-chip [8]. For the flip-chip case, the two 50-Ω transmission lines are connected using bumps. In Table 2, we show the performance of the vertical stacked via interconnect and bumped flip-chip.

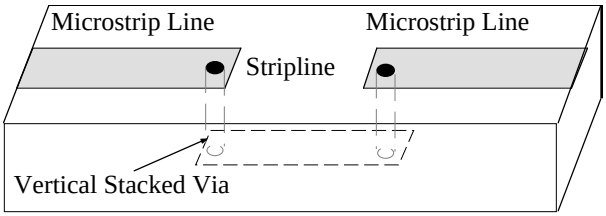


Figure 7. Schematic representation of a microstrip to stripline transition using vertical stacked via

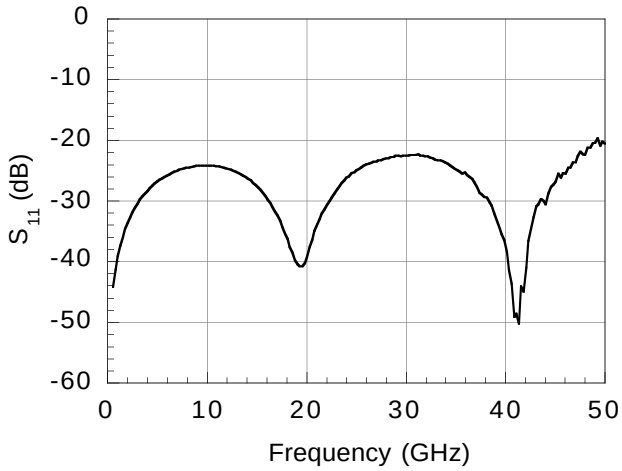


Figure 8. Measured return loss of the 50-Ω microstrip connected a 50-Ω stripline using the vertical stacked via interconnect

Table 1. Comparison of the return loss of the vertical stacked via and wirebond

Frequency (GHz)	Return loss of Via Stack (dB)	Return loss of Wirebond [7] (dB)
10	-24	-12
30	-22	-9
50	-20	-6

Table 2. Comparison of the return loss of two 50-Ω transmission lines connected using the vertical stacked via and flip-chip

Frequency (GHz)	Return loss of Via Stack (dB)	Return loss of Flip-chip [8] (dB)
10	-24	-21
30	-22	-17
50	-20	-15

Conclusion

We have presented the design and development of a multi-layer organic based MCM. We have developed the electrical model for the vertical stacked via and demonstrated that it has ultra low parasitics. We compare our vertical stacked via with wirebond and flip-chip to demonstrate its relative performance. We show that the measured return loss of two 50-Ω transmission lines is less than 20dB to 50GHz. We will present more results on a variety of interconnect and packaging architecture utilizing organic based MCM.

Acknowledgment

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References

[1] R. O. Carlson, C.W. Eichelberger, R.J. Wojnarowski, L.M. Levinson, and J.E. Kohl, "A High Density Copper/Polyimide Overlay Interconnection," *Proc. 8th IEPS Intl. Elec. Packaging Conf., pp. 793-804, 1988*

[2] P.D. Cooper, M.M. Fithian, R.J. Street, and W.P. Kornrumpf, "A C-Band GaAs MMIC T/R Module Using Microwave High-Density-Interconnect Technology," *Proc. of 18th Gov't Microcircuit Applications Conf.*, pp. 613-616, 1992

[3] V.B. Krishnamurthy, H.S. Cole, and T. Sitnik-Nieters, "Use of BCB in High Frequency MCM Interconnects," *IEEE Trans. Comp. Packaging, Manuf. Technol.*, Vol. 19, no. 1, pp. 42-47, Feb. 1996

[4] P. Cooper, P. Piacente, and R. Street, " Multichip-on-flex Plastic Encapsulated MHDI-Low Cost Substrateless Manufacturing for Microwave and Millimeterwave Modules", *IEEE MTT-S Digest*, pp. 219-222, June 1995.

[5] A. Pham, J. Laskar, V. Krishnamurthy, H.S Cole, and T. Sitnik-Nieters, "Ultra Low Loss Millimeter Wave MCM Interconnects", *IEEE 6th EPEP Digest*, 213-216, Oct. 1997.

[6] A. Pham, J. Laskar, J. Schappacher, " Development of On-wafer Microstrip Characterization Techniques," *IEEE 47th ARFTG Digest*, pp. 85-94, June, 1996

[7] T. Krems et al, "Millimeter-Wave Performance of Chip Interconnections Using Wire Bonding and Flip Chip," *IEEE MTT-S Digest*, Vol 1., pp 247-250, June 1996.

[8] T. Krems et al, "Advantages of Flip Chip Technology in Millimeter-Wave Packaging," *IEEE MTT-S Digest*, Vol. 1, pp 987-99-, June 1997.